Electronic Version
Stylesheet Version v1.1.1

Description

[METHOD OF DOPING SIDEWALL OF ISOLATION TRENCH]

Cross Reference to Related Applications

[0001] This application claims the priority benefit of Taiwan application serial no. 92122456, filed August 15, 2003.

Background of Invention

[0002] Field of the Invention

[0003] The present invention relates to a method of forming an isolation trench. More particularly, the present invention relates to a method of doping sidewalls of an isolation trench.

[0004] Description of the Related Art

[0005] The isolation region of a semiconductor device is a form of partition between neighboring field effect transistor for preventing the cross diffusion of currents. Putting up an isolation trench is an effective method of isolating devices. To form an isolation trench, a pad oxide layer and a

polishing stop layer are formed over a substrate. Thereafter, an anisotropic dry etching is carried out to form a trench in the semiconductor substrate. Finally, an insulation material is deposited to fill the trench serving as a device isolation structure.

[0006] Because the device that crosses over the isolation region and the corner of the active area has a relatively large electric field near the active area corner, sub-threshold leakage current has become an increasingly important problem for device operation. With the miniaturization of transistor devices and hence the reduction of channel width, the sub-threshold leakage current will be increasingly dominant resulting in the so-called narrow channel width effect. To reduce the severity of narrow channel width effect, US. Patent No. 5,960,276 disclosed a method of doping sidewalls of an isolation trench. Fig. 1 is a schematic cross-sectional view showing a conventional method of doping the sidewalls of an isolation trench. First, a pad oxide layer 101 and a polishing stop layer 102 is formed over a substrate 100. Thereafter, an anisotropic dry etching is carried out to form a trench 104 in the substrate 100. A photolithographic process is carried out to form a mask layer 109. The mask layer blocks the PMOS

region but exposes the NMOS region. Finally, a sidewall doping operation 106 is carried out to from a doped region 110 in the substrate 100 along the sidewalls of the trench 104.

[0007] After the sidewall doping operation 106, the doped region 110 not only spreads over the top section of the trench sidewall but also the lower and bottom section of the trench sidewall. The doped region 110 on the sidewall of the trench may overlap with the doped source/drain region of a subsequently formed transistor and increase their junction gradient. Hence, the electric field in the junction area will increase leading to a possible increase in junction leakage.

SUMMARY OF INVENTION

[0008] Accordingly, one object of the present invention is to provide a method of doping sidewalls of an isolation trench that can reduce sub-threshold leakage.

[0009] A second object of this invention is to provide a method of doping sidewalls of an isolation trench that can prevent junction leakage.

[0010] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a method

of doping sidewalls of an isolation trench. First, a substrate with at least a trench therein is provided. A blocking layer is formed within the trench. The top surface of the blocking layer is lower than the top surface of the substrate. Thereafter, a sidewall doping process is carried out to form a doped region in the substrate in the top section of the trench sidewall. Finally, the blocking layer is removed from the isolation trench.

[0011] This invention also provides a method of doping sidewalls of an isolation trench. The method can be applied to a substrate with a plurality of trenches. The substrate comprises a first region and a second region. First, a blocking layer is formed over the substrate to fill all the trenches. Thereafter, a patterned mold having at least a protruded section and at least a recess section is provided. The protruded section corresponds with the first region of the substrate and the recess section corresponds with the second region of the substrate. The patterned mold is pressed against the blocking layer so that the thickness of the blocking layer in the first region corresponding to the protruded section is lowered. After removing the patterned mold from the blocking layer, an etching operation is performed to remove a portion of the blocking layer

and expose the substrate on the upper section of the trench sidewall in the first region. A sidewall doping process is carried out to form a doped region in the substrate on the upper trench sidewall of the first region. Finally, the blocking layer is removed.

[0012] In this invention, the sidewall doping process is carried out with only the upper trench sidewall exposed. This is because all of the remaining areas including the bottom section of the trench and subsequent well area adjacent to the trench sidewall are blocked by the blocking layer. With the protection of the blocking layer, junction leakage resulting from an increased junction gradient due to an area overlap between a doped sidewall and a doped source/drain region of a subsequently formed transistor is prevented.

[0013] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0014] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The

drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0015] Fig. 1 is a schematic cross-sectional view showing a conventional method of doping the sidewalls of an isolation trench.

[0016] Figs. 2A through 2D are schematic cross-sectional views showing the progression of steps of the method of doping the sidewalls of an isolation trench according to a first preferred embodiment of this invention.

[0017] Figs. 3A through 3D are schematic cross-sectional views showing the progression of steps of the method of doping the sidewalls of an isolation trench according to a second preferred embodiment of this invention.

Detailed Description

[0018] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0019] Figs. 2A through 2D are schematic cross-sectional views showing the progression of steps of the method of doping

the sidewalls of an isolation trench according to a first preferred embodiment of this invention. As shown in Fig. 2A, a substrate 200 having at least a trench 204 is provided. The trench 204 is formed, for example, by forming a pad oxide layer 201 and a polishing stop layer 202 sequentially over the substrate 200 and etching the substrate 200 using the polishing stop layer 202 as a mask. Hence, the substrate 200 has a residual pad oxide layer 210 and a polishing stop layer 202. Thereafter, a blocking layer 208 is formed over the substrate 200 completely filling the trenches 204. The blocking layer 208 is formed, for example, by performing a spin-on coating or a chemical vapor deposition. Furthermore, the blocking layer 208 can be a photoresist layer, an anti-reflection coating (ARC), a spin-on dielectric layer or a doped dielectric layer. Before forming the blocking layer 208, a thermal oxide liner (not shown) may also be selectively formed over the exposed surface of the substrate 200 in the trenches 204.

[0020] As shown in Fig. 2B-1, a portion of the blocking layer 208 is removed to expose the upper section of the trench sidewall. Hence, the top surface of the blocking layer 208 is lower than the top surface of the substrate 200. An up-

per section of the blocking layer 208 is removed by performing an etching operation such as a reaction ion etching process or a wet etching process. Thereafter, a photolithographic process is selectively performed to form a mask layer 209 such as a photoresist layer that covers a second region 212b but exposes a first region 212a. The first region 212a and the second region 212b are distinguished by the type of MOS transistors fabricated thereon. For example, the first region 212a is an NMOS region and the second region 212b is a PMOS region. If the blocking layer 208 is a photoresist layer, a hard baking process must be carried out to harden the blocking layer 208 first. The step height for a conventional mask layer 109 on the surface of the substrate 100 as shown in Fig. 1 includes the pad oxide layer 101, the polishing stop layer 102 and the depth of the trench 104. Compared with the convention method, the step height of the mask layer 209 is considerably lowered because the trenches 204 have already been filled by the blocking layer 208 in this invention. In other words, the process window for performing the photolithographic process is increased. In addition, if the blocking layer 208 is an anti-reflection coating (ARC), the amount of reflection during a photo-exposure opera-

tion can be reduced so that the process window for forming the mask layer 209 is further increased.

[0021] Aside from the step carried out as in Fig. 2B-1, an alternative step as shown in Fig. 2B-2 can be used. First, a patterned mask layer 209 such as a photoresist layer is formed over the blocking layer 208 within the second region 212b. Using the patterned mask layer 209 as an etching mask, a reactive ion etching or a wet etching operation is performed to remove a portion of the blocking layer 208. Ultimately, the upper sidewall of the trench 204 in the first region 212a is exposed and the top surface of the remaining blocking layer 208 is lower than the top surface of the substrate 200. The step height of the mask layer 209 is considerably lowered compared with the mask layer formed by the conventional technique because the trenches 204 have already been filled by the blocking layer 208 in this invention. In other words, the process window for performing the photolithographic process is increased. In addition, if the blocking layer 208 is an anti-reflection coating (ARC), the amount of reflection during a photo-exposure operation can be reduced so that the process window for forming the mask layer 209 is further increased.

[0022] Thereafter, as shown in Figs. 2C-1 and 2C-2, a sidewall doping process 206 such as an ion implantation (I/I) is carried out to form a doped region 210 in the substrate 200 on the upper sidewall of the trench 204. The type of ions used in the ion implantation process is complementary to the doping configuration of the source/drain terminal of a subsequently formed transistor. For example, if the subsequently formed transistor is an NMOS transistor, P-type ions (for example, boron ions) are used in the ion implantation. Furthermore, the implantation depth is shallower than the doped source/drain region of the subsequently formed transistor. The ion implantation is typically carried out using an implantation energy level between 5 to 40 KeV, a dosage between 5E12 to 1E14 ions/cm^2 and a slant angle relative to the perpendicular direction between 5 to 30°.

[0023] Finally, as shown in Fig. 2D, the blocking layer 208 and the mask layer 209 (refer to Figs. 2C-1 and 2C2) within the trench 204 are removed in preparation for subsequent semiconductor fabrication processes.

[0024] Figs. 3A through 3D are schematic cross-sectional views showing the progression of steps for doping the sidewalls of an isolation trench according to a second preferred

embodiment of this invention. In the second embodiment of this invention, a nanoimprint lithographic technique is applied, a detailed description of which is disclosed in U.S. Patent No. 6,482,742 and is included herein by reference. First, as shown in Fig. 3A, a substrate 300 with a residual pad oxide layer 301 and a polishing stop layer 302 thereon is provided. The substrate 300 comprises a first region 312a and a second region 312b. The first region 312a of the substrate 300 also has a plurality of trenches 304. Different types of MOS transistors can be formed on the first region 312a and the second region 312b. For example, NMOS transistors can be formed on the first region 312a and PMOS transistors can be formed on the second region 312b. Thereafter, a blocking layer 308 is formed over the substrate 300 completely filling the trenches 304. The blocking layer 308 is formed, for example, by a performing a spin-on coating or a chemical vapor deposition. Furthermore, the blocking layer 308 can be a photoresist layer, an anti-reflection coating (ARC), a spin-on dielectric layer, a thermoplastic polymer, a thermal-hardening layer or a radiation-hardening layer. Before forming the blocking layer 308, a thermal oxide liner (not shown) may also be selectively formed over the exposed

surface of the substrate 300 in the trenches 304.

[0025] A patterned mold 314 comprising a main body 316 with a protruded section 318 and a recess section 320 underneath the main body 316 is provided. The protruded section 318 corresponds with the first region 312a of the substrate 300 and the recess section 320 corresponds with the second region 312b of the substrate 300.

[0026] As shown in Fig. 3B, the patterned mold 314 is pressed against the blocking layer 308 so that the thickness of the blocking layer 308 in the first region 312a corresponding to the protruded section 318 is reduced and the pattern in the mold 314 is transferred to the blocking layer 308. Furthermore, the substrate 300 can be heated or irradiated to harden the blocking layer 208 when the mold 314 is still pressed against the blocking layer 308. Afterwards, the patterned mold 314 is removed from the blocking layer 308.

[0027] As shown in Fig. 3C, an etching operation such as a reactive ion etching or a wet etching operation is performed. After the etching operation, a portion of the blocking layer 308 is removed and the upper sidewall of the trench 304 within the first region 312a is exposed. A sidewall doping process 306 such as an ion implantation (I/I) is carried out

to form a doped region 310 in the substrate 300 on the upper sidewall of the trench 304. The type of ions used in the ion implantation process is complementary to the doping configuration of the source/drain terminal of a subsequently formed transistor. For example, if the subsequently formed transistor is an NMOS transistor, P-type ions (for example, boron ions) are used in the ion implantation. Furthermore, the implantation depth is shallower than the doped source/drain region of the subsequently formed transistor. The ion implantation is typically carried out using an implantation energy level between 5 to 40 KeV, a dosage between 5E12 to 1E14 ions/cm^2 and a slant angle relative to the perpendicular direction between 5 to 30°.

[0028] Finally, as shown in Fig. 3D, the blocking layer 308 (refer to Figs. 3C) within the trenches 304 are removed in preparation for subsequent semiconductor fabrication processes. Compared with the double layered structure (the blocking layer 208 and the mask layer 209) in the first embodiment, the second embodiment in association with the nanoimprint technique only requires a single blocking layer 308 (as shown in Fig. 3C). Thus, the number of processing steps in fabricating the isolation trench

is further reduced.

[0029] In summary, one major aspect of this invention is the blocking of the bottom section and the trench sidewall neighboring other well areas during the sidewall doping process. Hence, there is no overlapping with the doped source/drain region of a subsequently formed transistor to cause junction leakage. Moreover, the increase in sub-threshold leakage current due to devices crossing over the isolation region and the corner of the active area is prevented.

[0030] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.